REMARKS:

Claims 23-34 are currently pending in the present application. Claims 23 and 25-27 were rejected under 35 U.S.C. 102 (a) as being unpatentable over Harington III (US 5,688,722) in view of Kusonoki (US 6,066,880). Claims 28-31 were objected to as being dependant upon a rejected base claim, but noted to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for this indication of allowable subject matter. In this amendment, independent claim 23 has been rewritten to include the limitations of claim 28, with claim 28 being cancelled. Additional changes have been made to claim 23 as well as to claims 26-27 and 29 to provide consistency in nomenclature. No new matter has been added. Claims 32-34 have also been added. Support for the new claim may be found throughout the specification, including FIGS. 3-9B and the original claims. No new matter is introduced by these amendments.

Claim Rejections Under 35 USC 103:

Claims 23 and 25-27 were rejected under 35 U.S.C. 102 (a) as being unpatentable over Harington III (US 5,688,722) in view of Kusonoki (US 6,066,880). Claim 23 has been amended to include limitations from claim 28, previously noted by the Examiner to contain allowable subject matter and thus the rejection is believed to be overcome thereby. More specifically, Harington in combination with Kusonoki do not teach or suggest the invention as recited in claim 23 including the predetermined dopant positioned at a selected level in the second region of the substrate below the gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer when the second gate is biased with respect to the substrate and the buried channel is partially depleted of charge carriers, to increase the effective gate oxide thickness of the second device, the buried channel being doped with a predetermined dopant of a first conductivity type in a substrate region of a second conductivity type. Thus for at least these reasons, applicant submits that claim 23 is patentable over the art of record.

Claim 32 is submitted to be patentable over the art of record for the same reasons as discussed above with respect to claim 23. In specific, the combination of Harington and Kusunoki fails to teach or suggest the invention as recited in claim 32

for the reason that no suggestion is made as to configuring the second device such that the substrate portions above the buried channel act as a supplemental gate dielectric layer when the gate is biased with respect to the substrate and the buried channel is partially depleted of charge carriers, to increase an effective gate oxide thickness of the second device. Kusonoki, in the passage cited by the Examiner (col. 8, lines 4-10), provides a variation in the virtual thickness of the insulation layer with a change of the depletion layer formed on the second gate electrode. Thus, Kusonoki refers to using the depletion layer formed in the gate, not in the substrate (under the gate oxide) as required in the invention claimed in claim 32. Likewise, applicants submit that FIGS. 68-79 provide no support for using a buried channel in the substrate to increase the effective gate oxide thickness since the accompanying descriptions refer generally to conventional channel doping in insulated gate transistors. Further, the discussion relating to FIGS. 42-46 (in Kusonoki) refer to adjusting the impurity concentration of the gate electrode to regulate the depletion layer width (col. 23. lines 25-40), not by implanting the channel and configuring the channel in a biased condition as required in claim 32. That is. Kusonoki teaches that a higher breakdown voltage can be obtained by adjusting the depletion layer width of the gate by controlling the impurity concentration of the gate electrode. This is distinguishable form the invention as recited in claim 32 in that adjusting the impurity concentration layer in the doped gate doesn't teach or suggest adjusting and biasing the channel implant in the substrate to convert the substrate portions above the buried channel into a supplemental gate dielectric layer. As acknowledged by the Examiner on page 3 of the office action, Harington also does not disclose the dopant concentration acting to provide a supplemental gate dielectric layer to increase effective dielectric thickness. For at least the foregoing reason, applicants submit that claim 32 is allowable over the art of record.

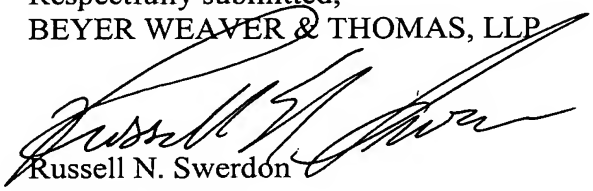
Claims 24-27 and 29-31 and 33-34 are dependant claims that are believed to be patentable over the art of record for at least their dependency from an allowable independent claim. Moreover, the dependent claims recite additional limitations, and are therefore allowable for these reasons as well. The allowability of subject matter captured in certain dependant claims was noted by the Examiner in the discussion of allowable subject matter and objectionable claims. In light of the above distinctions in the independent claims and the concession by the Examiner as to allowable subject

matter in claims 29-31, further discussion of the dependent claims is deemed unnecessary.

Conclusion

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.
If any fees are due over and above the fees provided with the amendment, such fees may be charged to deposit account No. 12-2252 (client docket 01-721).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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